REMARKS

Claims 1-35 stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion. Claims 21 and 30 are cancelled herein, thus, claims 1-20, 22-29, and 31-35 are all the claims pending in the application.

I. The Prior Art Rejections

Claims 1-6 and 8-13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Okitaka (U.S. Patent No. 6,343,366). Claims 7 and 14-21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Okitaka, in view of Hirabayashi (U.S. Publication No. 2002/0170003), in further view of Tran (U.S. Patent No. 5,961,634). Claims 22-35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Okitaka, Hirabayashi and Tran either alone or in combination. Applicants respectfully traverse these rejections based on the following discussion.

A. Rejection of independent claims 1, 8, 15, 22 and 29.

The Applicants respectfully submit that Okitaka does not teach or suggest the following features of claims 1, 8 and 15 or the similar features of claims 22 and 29: (1) "a BIST logic controller that is separate from said embedded memory arrays, is adapted to operate at a lower frequency than said embedded memory arrays, and is further adapted to perform test functions common to all of said embedded memory arrays at said lower frequency"; (2) "a plurality of blocks of test logic in communication with said BIST logic controller"; (3) "wherein each one of said blocks is incorporated into a corresponding one of said embedded memory arrays under test, is adapted to operate at a same frequency as

said corresponding one of said embedded memory arrays, and is further adapted to perform test functions unique to said corresponding one of said embedded memory arrays at said same frequency"; (4) "wherein said same frequency comprises a higher frequency relative to said lower frequency of said BIST logic controller" (5) "wherein said BIST logic controller is further adapted to communicate, to each of said blocks, instructions at said lower frequency"; and (6) "wherein said each of said blocks is further adapted to locally process said instructions at said higher frequency."

More particularly, Okitaka teaches four embodiments (see Figures 2-5 respectively) of a BIST circuit designed for large scale integrated (LSI) memory (e.g., DRAM or SRAM). Each embodiment of Okitaka comprises a BIST controller 1 for controlling a self test operation of a memory array (i.e., the one memory array 51). As illustrated in Figures 2-5, the BIST controller 1 is separate from the memory array 51. The different embodiments of the BIST circuit of Okitaka differ with regard to incorporation of other features, such as a GO/NG register 4, an error information register 5, a selector 6, a repair code generator/register 7 and a self repair circuit 8 (see discussion of First Embodiment beginning at col. 4, line 29; see discussion of Second Embodiment beginning at col. 6, line 7; see discussion of Third Embodiment beginning at col 7, line 48; and see discussion of Fourth Embodiment beginning at col. 9, line 24). However, in each embodiment the single BIST controller 1 is connected to a single memory array. It does not control BIST functions for multiple different memory arrays.

Contrarily, in the claimed invention, a hybrid BIST architecture is disclosed for use with multiple different memory arrays. That is, BIST functionality is segmented

between a single lower frequency remote BIST controller that performs common test functions and multiple higher frequency blocks of test logic that locally perform test functions unique to corresponding memory arrays (see paragraphs [0028-0030]). This hybrid architecture enables testing of different types, sizes and/or frequencies of memory arrays in parallel.

The Office Action provides that "Okitaka substantially teaches a hybrid built-in self test (BIST) architecture (figure 5) for embedded memory arrays (Figure 5 #51) that segments FIST functionality into remote lower-speed executable instructions (Figure 4#1) and local higher-speed executable instructions (Figure 5 #1)". The Applicants respectfully disagree. As mentioned above, each of the embodiments of Okitaka discloses a single BIST controller 1 connected (via a test pattern generator 2) to a single memory array 51. As illustrated in Figures 5 and 1, the BIST controller 1 is separate from the single memory array 51 and no blocks of test logic, separate from the BIST controller, are disclosed as incorporated into the single memory array 51. Thus, Okitaka does not teach or disclose a remote BIST controller that is in communication with blocks of test logic that are each incorporated into a corresponding one of multiple embedded memory arrays.

Additionally, Figure 4 and Figure 5 illustrate different embodiments of the same BIST structure such that item #1 in Figure 4 and in Figure 5 corresponds to the same component. Specifically, the description of the Fourth embodiment discusses a variation over the Third Embodiment (i.e., item #9), but provides at col. 9, lines 40-45 that "Other components in the BIST circuit as the fourth embodiment are the same of the components

in the BIST circuit as the third embodiment, the same reference numbers are used for the same components, and the explanation of them is therefore omitted here for brevity." Thus, since item #1 is the same feature in Figures 4 and 5, it can not properly be cited as teaching a BIST architecture that segments BIST functionality into remote lower-speed executable instructions (cited in the Office Action as being taught by Figure 4 #1) and local higher-speed executable instructions (cited in the Office Action as being taught by Figure 5 #1).

The Office Action further provides that Okitaka teaches "the architecture comprising: a standalone BIST logic controller (Figure 4 #1) operating at a lower frequency and being adapted to communicate with a plurality of embedded memory arrays using a BIST instruction set (columns 9-10, lines 63-9); and a block of higher speed test logic (Figure 5 #9) incorporated into each embedded memory array under test (Figure 5 #51) and being adapted to locally process BIST instructions received from said standalone BIST logic controller at a higher frequency than said lower frequency (column 9, lines 35-40)." The Applicants respectfully disagree.

Each of the embodiments of Okitaka discloses a single BIST controller 1 connected (via a test pattern generator 2) to a single memory array 51. As discussed above, Okitaka does not teach or disclose a single BIST controller that is in communication with blocks of test logic that are each incorporated into a corresponding one of multiple embedded memory arrays. Thus, Okitaka necessarily does not teach or suggest that the BIST controller is adapted to perform test functions common to all of the embedded memory arrays. Nor does Okitaka teach or suggest that each block of test

logic incorporated into each embedded memory array is adapted to perform test functions unique to its corresponding embedded memory.

Additionally, Okitaka does not teach or suggest a BIST controller that communicates instructions to a memory array (or a block of test logic therein). Specifically, item #1 in each of the embodiments of Okitaka refers to a BIST controller that indicates the commencement of the self-test operation for the memory cell array 51 by generating and outputting a control signal to a test pattern generator 2. Then, the test pattern generator 2 generates and writes test pattern data to the memory array. Nowhere in Okitaka does it teach or disclose that instructions are communicated from the BIST controller to the memory array, much less to a block of test logic incorporated into the memory array.

Furthermore, while the Fourth Embodiment of Okitaka does include a phase locked loop for varying a clock signal in order to increase the frequency of the clock signal input into the BIST controller 1, it does not disclose a clock multiplier that is incorporated into a block of test logic in an embedded memory array in order to allow instructions received by the memory array at a lower frequency to be locally processed at a higher frequency. More specifically, the Fourth Embodiment (see Figure 5) is similar to the other embodiments but further comprises a phase locked loop (PLL) 9 (see col. 9, lines 34-40) for inputting an external clock signal provided from an external device (omitted from FIG. 5) and for generating an internal clock signal, whose frequency is higher than that of the received one, based on the received external clock signal, and then for outputting the internal clock signal to internal circuits such as the BIST circuit in the

LSI." Thus, Okitaka only discloses a BIST controller 1 that operates at the same frequency as the memory array 51.

The Office Action acknowledges Okitaka does not disclose a frequency multiplier in a block of test logic but provides that "It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the PLL in the Memory Cell Array after the BIST, since it has been held that rearranging parts of an invention involves only routine skill in the art." The Applicants, however, submit that even if it were obvious to rearrange the order of components in the Okitaka circuit so that the PLL is after the BIST controller, the claimed features of the invention would still not be taught or made obvious. Specifically, neither the components of the Okitaka circuit, nor rearrangement thereof, would teach or make obvious communicating instructions at a lower frequency to blocks of test logic incorporated into an embedded memory array or processing those instructions locally at a higher frequency.

Therefore, amended independent claims 1, 8, 15, 22 and 29 are patentable over Okitaka. Further, dependent claims 2-7, 9-14, 16-20, 23-28 and 31-35 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

B. Rejection of independent claims 8, 15 and 29.

The Applicants further respectfully submit that Okitaka does not teach or suggest

the following feature of claims 8 and 15 or the similar feature of claim 29: "a bus connecting said BIST logic controller to each of said blocks of test logic so as to allow communication from said BIST logic controller to said blocks, wherein said bus is adapted to operate at said lower frequency".

More particularly, the Office Action provides Okitaka discloses "a bus connecting said remote BIST logic controller to said embedded blocks of test logic (Figure 5 signal between #1, #2, & #3, col. 9, lines 64-67, the BIST connected indirectly but the BIST is essentially transmitting the signal which ultimately initiates the self-test mode)..." The Applicants respectfully disagree. Okitaka does not disclose a bus. Specifically, those skilled in the art will recognize that a bus in this context is a parallel circuit that connects multiple components to any other component. The connections between the different components 1, 2, 51, 3, etc. of Okitaka are direct connections. That is, the BIST controller 1 of Okitaka outputs a control signal to the test generator 2 indicating the commencement of the self test operation. Then the test pattern generator 2 generates and writes test pattern data to the memory array 51 (see col. 5, lines 4-17). The signal output by the BIST controller 1 is not received by the memory array 51, much less by a block of test logic incorporated into the memory array 51.

Therefore, amended independent claims 8, 15 and 29 are patentable over Okitaka. Further, dependent claims 9-14, 16-20 and 31-35 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define. Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings, and no

new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-20, 22-29, 31-35, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 3/29/07

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